WHAT IS CLAIMED IS:

1. A phase-error suppressor for use with a plurality of transistors having a common source coupled to a current generator and configured to receive signals at a frequency, comprising:

an inductor, coupled between said common source and said current generator, configured to resonate proportionally to said frequency with a first capacitance associated with said plurality of transistors.

2. The phase-error suppressor as recited in Claim 1 wherein said plurality of transistors and said current generator form a portion of a system selected from the group consisting of:

a quadrature oscillator buffer,

a quadrature oscillator, and

a quadrature mixer.

3. The phase-error suppressor as recited in Claim 1 wherein said inductor and said first capacitance resonate at twice said frequency.

4. The phase-error suppressor as recited in Claim 1 wherein said first capacitance is dominated by a base-to-emitter capacitance of at least one of said plurality of transistors.

5. The phase-error suppressor as recited in Claim 1 further comprising a capacitor coupled to said inductor and coupled in parallel to said current generator, said capacitor being configured to shunt said inductor to ground at a selected radio frequency (RF).

6. The phase-error suppressor as recited in Claim 1 wherein said frequency is at least three GHz.

7. The phase-error suppressor as recited in Claim 1 where said signals are four periodic local oscillator signals having a 90 degree phase difference.

8. A method of suppressing a phase-error for use with a plurality of transistors having a common source coupled to a current generator and configured to receive signals at a frequency, comprising:

coupling an inductor in series between said common source and said current generator; and

causing said inductor to resonate proportionally at said frequency with a first capacitance associated with said plurality of transistors thereby suppressing a phase-error associated with said signals.

9. The method as recited in Claim 8 wherein said plurality of transistors and said current generator form a portion of a system selected from the group consisting of:

a quadrature oscillator buffer,

a quadrature oscillator, and

a quadrature mixer.

10. The method as recited in Claim 8 wherein said inductor and said first capacitance resonate at twice said frequency.

11. The method as recited in Claim 8 wherein said first capacitance is dominated by a gate-to-source capacitance of said transistors.

12. The method as recited in Claim 8 further comprising coupling a capacitor to said inductor and in parallel to said current generator, said capacitor shunting said inductor to ground at a selected radio frequency (RF).

13. The method as recited in Claim 8 wherein said frequency is at least three GHz.

14. The method as recited in Claim 1 wherein said signals are four periodic local oscillator signals having a 90 degree phase difference.

15. An image-rejecting down-converter for use with a radio frequency (RF) receiver, comprising:

a local oscillator (LO) configured to provide an in-phase signal and a quadrature-phase signal at a frequency;

a quadrature mixer configured to combine said in-phase and said quadrature-phase signals with a RF signal; and

a quadrature oscillator buffer, coupled between said LO and said quadrature mixer, including:

a plurality of transistors having a common source coupled to a current generator and configured to receive one of said in-phase and said quadrature-phase signals from said LO at said frequency; and

an inductor, coupled between said common source and said current generator configured to resonate proportionally to said frequency with a first capacitance associated with said plurality of transistors to suppress a phase-error between said in-phase and said quadrature-phase signals.

16. The image rejecting down-converter as recited in Claim 15 wherein said quadrature mixer, includes:

a second plurality of transistors having a second common source coupled to a second current generator and configured to receive one of said in-phase and said quadrature-phase signals at said frequency; and

a second inductor, coupled between said second common source and said second current generator, configured to resonate proportionally to said frequency with a second capacitance associated with said second plurality of transistors to suppress phase-error between said in-phase and said quadrature-phase signals.

17. The image rejecting down-converter as recited in Claim 15 wherein said inductor and said first capacitance resonate at twice said frequency.

18. The image rejecting down-converter as recited in Claim 15 wherein said first capacitance is dominated by a base-to-emitter capacitance of at least one of said plurality of transistors.

19. The image rejecting down-converter as recited in Claim 15 wherein said quadrature oscillator buffer further comprises a capacitor, coupled to said inductor and coupled in parallel to said current generator, said capacitor being configured to shunt said inductor to ground at a selected RF.

20. The image rejecting down-converter as recited in Claim 15 wherein said frequency is at least three GHz.

21. The image rejecting down-converter as recited in Claim 15 where said in-phase and said quadrature-phase signals are four periodic local oscillator signals having a 90 degree phase difference.